IN THE CLAIMS:

1. A method for moving a data string within a cache memory system, the method comprising:

reading a cache line from a data cache, the cache line containing at least a portion of a data string and having a starting source address;

shifting the cache line a selected amount;

storing the shifted cache line in a first destination cache line in the data cache, the shifted cache line having a starting destination address; and

modifying a cache tag value associated with the first destination cache line to reflect a location of the data string in a main memory.

2. The method of Claim 1, further comprising:

storing in a register data shifted out of the cache line during the shift operation;

reading from the data cache a second cache line containing at least a portion of the data string;

shifting the second cache line said selected amount;

filling the shifted second cache line with the data stored in the register during said shifting; and

storing the shifted second cache line in a second destination cache line in the data cache.

- 3. The method of Claim 2, wherein the register has a capacity that is one byte less than the size of the cache line.
- 4. The method of Claim 1, wherein shifting the cache line is performed with a barrel shifter.
- 5. The method of Claim 1, wherein said selected amount is an amount equal to a change in offset between the starting source address and the starting destination address.
- 6. The method of Claim 1, further comprising marking the first destination cache line as having been modified.
 - 7. The method of Claim 1, further comprising performing a snoop cycle.

- 8. The method of Claim 1, further comprising writing to the main memory data stored in the first destination cache line prior to the data string move.
- 9. The method of Claim 1, wherein the main memory comprises a DRAM circuit.
- 10. The method of Claim 1, wherein the data cache comprises a Level 1 cache.
- 11. The method of Claim 1, wherein the acts of reading, shifting and storing are pipelined.
- 12. A cache memory system for moving a data string, the cache memory system comprising:

a cache memory comprising:

and

a cache data memory configured to store a data string; and a cache tag memory associated with the cache data memory;

a shifter coupled to the cache memory, the shifter being configured to shift an entire cache line containing at least a portion of the data string in a single processor cycle, the cache data memory being configured to store the shifted cache line in a destination cache line.

- 13. The cache memory system of Claim 12, wherein the shifter comprises a barrel shifter.
- 14. The cache memory system of Claim 12, wherein the shifter is further configured to shift the entire cache line an amount equal to a change in offset between a starting source address of the cache line and a starting destination address of the shifted cache line.
- 15. The cache memory system of Claim 12, further comprising a register coupled to the shifter for storing data shifted out of the shifter during shift operations.
- 16. The cache memory system of Claim 15, wherein the register is configured to store one byte less than the size of the cache line.
- 17. The cache memory system of Claim 12, further comprising a processor configured to mark the destination cache line as having been modified.

- 18. The cache memory system of Claim 12, further comprising a memory controller configured to perform a snoop cycle.
- 19. The cache memory system of Claim 12, further comprising writing the data stored in the destination cache line to a main memory prior to storing the shifted cache line in the destination cache line.
- 20. The cache memory system of Claim 12, wherein the cache memory comprises a Level 1 cache.
- 21. A method of reassigning data from a first memory location to a second memory location comprising:

reading a cache line containing at least a portion of a data string from a data cache;

shifting the cache line a selected amount; and storing the shifted cache line in the data cache.

22. The method of Claim 21, further comprising:

storing data shifted out of the cache line during said shift operation in a register;

reading a second cache line containing at least a portion of the data string from the data cache;

shifting the second cache line said selected amount;

filling the second cache line with the data stored in the register during said shifting; and

storing the second cache line in the data cache.

- The method of Claim 22, wherein a capacity of the register is less than the size of the cache line.
- 24. The method of Claim 21, wherein shifting the cache line is performed with a barrel shifter.
- 25. The method of Claim 21, wherein said selected amount is an amount equal to a change in offset between a source address of the cache line and a destination address of the shifted cache line.
- 26. The method of Claim 21, further comprising marking the shifted cache line as modified.

- 27. The method of Claim 21, further comprising performing a snoop cycle.
- 28. The method of Claim 21, further comprising modifying a cache tag value associated with the shifted cache line.
- 29. The method of Claim 21, further comprising writing a portion of the data string to a main memory without writing the portion to the data cache.
- 30. The method of Claim 29, wherein the main memory comprises a DRAM circuit.
- 31. The method of Claim 21, wherein the data cache comprises a Level 1 cache.
- 32. The method of Claim 21, wherein the acts of reading, shifting and storing are pipelined.
 - 33. A cache memory comprising:
 - a data memory; and
 - a barrel shifter coupled to the data memory, the barrel shifter being configured to shift an entire cache line in a single processor cycle.
- 34. The cache memory of Claim 33, further comprising a register coupled to the barrel shifter for storing data shifted out of the barrel shifter during shift operations.
- 35. The cache memory of Claim 34, wherein the register has a capacity that is less than the size of the cache line.
- 36. The cache memory of Claim 33, wherein the barrel shifter is further configured to shift the entire cache line an amount equal to the change in offset between a source address and a destination address of the cache line.
- 37. The cache memory of Claim 33, further comprising a processor configured to mark the cache line as having been modified.
- 38. The cache memory of Claim 33, further comprising a memory controller configured to perform a snoop cycle.
- 39. The cache memory of Claim 33, wherein the data memory comprises a Level 1 cache.
- 40. The cache memory of Claim 33, wherein at least a portion of the data is written to a main memory instead of to the data memory.

- 41. The cache memory of Claim 40, wherein the main memory comprises a DRAM circuit.
 - 42. A processor comprising:
 a cache memory;
 means for reading a cache line from the cache memory;
 means for shifting the cache line a selected amount;
 means for storing data shifted out of the cache line; and

write circuitry for writing the shifted cache line to the cache memory.

- 43. The processor of Claim 42, wherein the means for shifting comprises a barrel shifter.
- 44. The processor of Claim 42, wherein said selected amount is an amount equal to the difference in offset between a source address of the cache line and a destination address of the shifted cache line.
- 45. The processor of Claim 42, wherein the means for storing data shifted out of the cache line has a capacity that is less than the size of the cache line.
- 46. The processor of Claim 42, wherein the means for storing data shifted out of the cache line comprises a register.
- 47. The processor of Claim 42, further comprising processing means for marking the shifted cache line as having been modified.
- 48. The processor of Claim 42, further comprising a means for performing a snoop cycle.
- 49. The processor of Claim 42, wherein the cache memory comprises a Level 1 cache.
- 50. The processor of Claim 42, wherein the means for reading, the means for shifting and the write circuitry are coupled to operate in a pipeline configuration.
- 51. The processor of Claim 50, wherein the cache lines are moved at a rate of one cache line per processor cycle.